ICF-6700W

FM/AM MULTI BAND RECEIVER

Canadian Model
US Model
AEP Model
UK Model
E Model

SUPPLEMENT

File this supplement with the service manual.

No. 1
December, 1978

I. RECEPTION CIRCUIT

Fig. 1 is a block diagram of the equipment. Only the main parts are indicated to clearly illustrate the operation of the system. The basic system is the same as that of Sony's other medium-priced sets, except for the digital display of the received frequency. Consequently, it is very different from others like the ICF-6800W with synthesizers. It consists of advanced circuits giving high efficiency. These include a double super heterodyne circuit with I-Fs at 10.7 MHz and 455 kHz, a balanced type first frequency mixer, a preselector with high gain over a wide frequency range, a low frequency filter to enable easy listening to SSB, an FET RF amplifier that withstands noise and even an FET RF stage in the MW band.

Below is a brief explanation of how these circuits process the received signals.

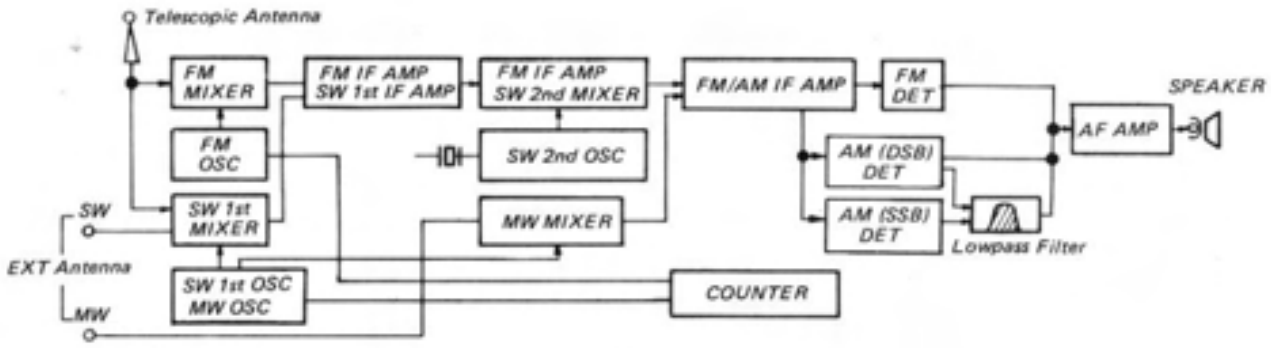


Fig. 1

SONY
SERVICE MANUAL

1. SW bandpass filter

A bandpass filter is installed in the SW external antenna terminal input circuit. This filter prevents large-amplitude signals of unwanted frequencies from getting into the high-frequency amplifier. The filter is not installed at the rod antenna, however, because the impedance of the rod antenna is high enough to reject undesired large-amplitude signals. In addition, the filter would be less effective because of the high and frequency-dependent impedance of the rod antenna.

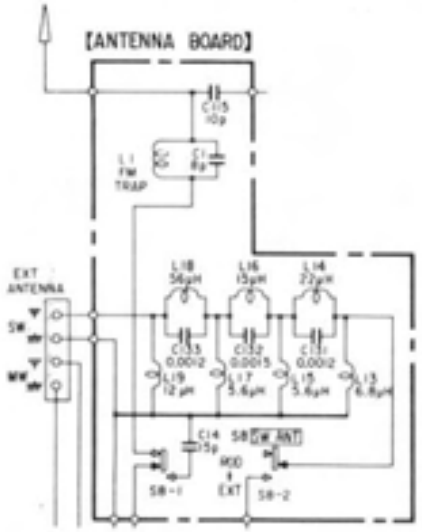


Fig. 2

2. Preselector

Preselectors are installed at both the input and output sides of RF amplifier Q4 and are synchronized. These are the same as the RF amplification circuits of regular type of receivers, but in order to maintain high efficiency over a wide range of frequencies and also to simplify the system, they are designed to be operated separately from the main dial. Moreover, L and C are set to be variable since a wide range of frequencies are to be covered.

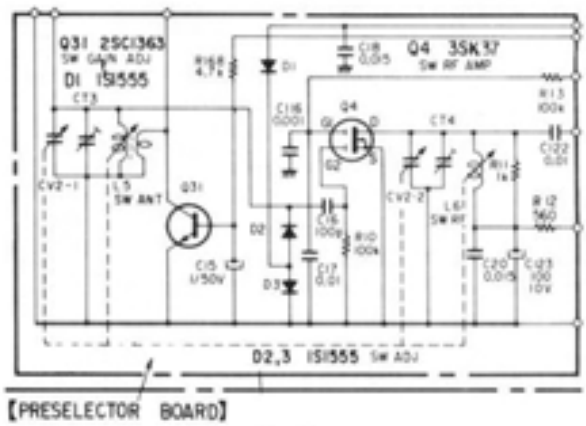


Fig. 3

3. High frequency gain adjustment See Fig. 3 and 4.

RV1 controls the impedances of Q31, D2 and D3 which are also the input impedance of RF amplifier Q4. It also controls impedances D4, D6 of the antenna circuit in the MW band and results in varying the RF gain in the MW band as well. When RV1 is at the maximum gain position, AGC voltage is applied to D2, D3, D4 and D6.

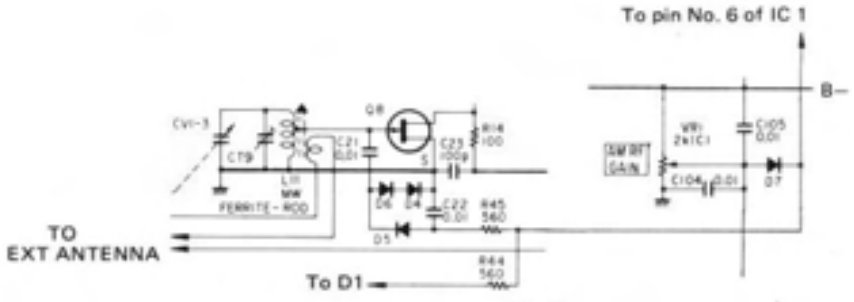


Fig. 4

4. SW primary frequency mixer (Q16, 17)

This balanced type frequency mixer consists of two 2SK23As. A characteristic of this type of frequency mixer is that signals entering from the balanced side are not, as a rule, transmitted to the output side. The received signal amplified by Q4 enters the balanced side. Applying the received signal to the balanced side makes it low in noise even when spurious waves of different frequencies are brought into the frequency mixer. This becomes quite effective for spurious waves which are the same as the first I-F 10.7 MHz. A variable resistor is installed in the source circuit so that the gains of Q16 and Q17 are simulaneously adjusted for the best balance. Local oscillation output is transmitted to the source. This frequency mixer transfers the received frequency to 10.7 MHz to enter the FM 1-F amplifier. Setting the first I-F at 10.7 MHz means that the circuit can be used for FM and, since the frequency is high, an outstanding image rejection rate is obtained.

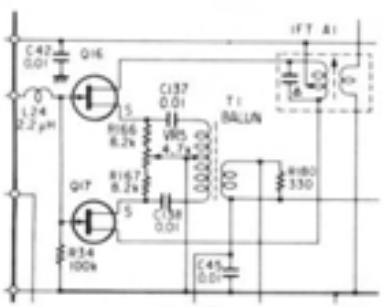


Fig. 5

5. SW second frequency mixer (Q10)

This frequency mixer also operates as an FM I-F amplifier. For SW, by changing the bias it can be used as a second frequency mixer. This also transfers 10.7 MHz to the second I-F of 455 kHz. A local oscillator signal of high stability from a crystal oscillator is put into the emitter. The frequency of the local oscillator is fixed at 10.245 MHz. The output of the second frequency mixer enters IC1 by way of CFT and CFU to be amplified.

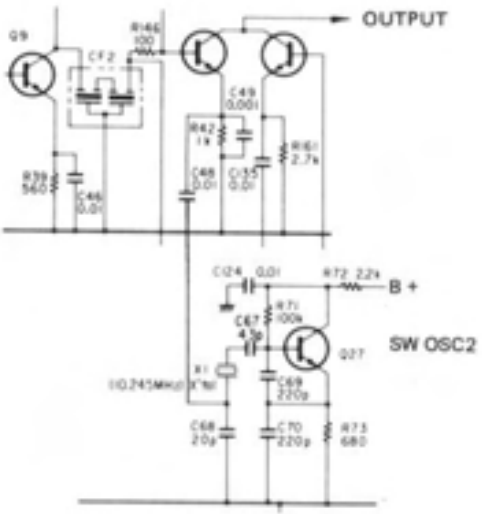


Fig. 6

6. SW second 1-F amplifier (IC1)

This IC contains not only an AM I-F amplifier but also an FM I-F amplifier, an AGC circuit, a meter circuit, etc.

7. Wave detector (D14–D16)

D14 and D15, D16 are wave detector diodes for DSB and SSB respectively. The detector for SSB is an ordinary balanced product detector. LSB and USB are selected by using S2-2 and C134 to shift the frequency by 2 kHz. This is performed by adjusting the core of L12 so that reproduced frequencies of LSB and USB become identical after receiving non-modulated waves accurately at the DSB position. The wave detector for DSB is a conventional type.

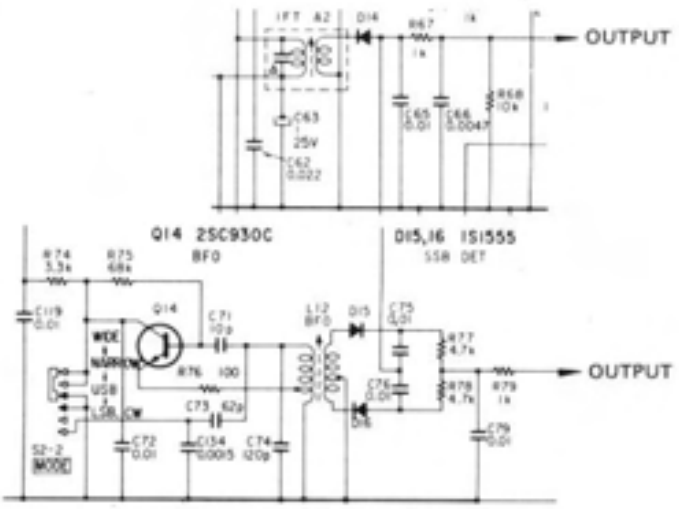


Fig. 7

8. Low-frequency filter (Q15, Q46, Q47)

It is more important for SSB receivers to reproduce sound easy to understand, rather than high fidelity sound, for this reason after the signal is detected it is passed through the bandpass filter to cut off unwanted frequencies and noise. The dedector output in SSB operation is usually lower than that of DSB, and thus the filter produces some gain. Even for DSB, this filter cuts off the high and low range of frequencies so that the sound is easy to understand. This filter has a peak at approximately 1 kHz and is approximately −20 dB at 150 Hz and 2 kHz. After this filter, the signal is amplified by the AF amplifier and is sent to the speakers.

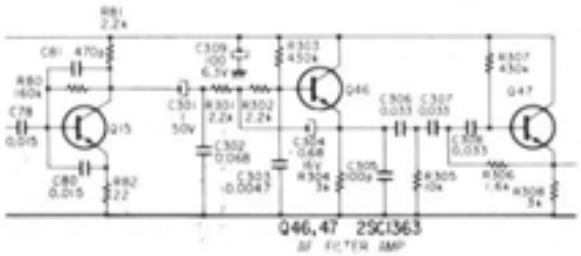


Fig. 8

II. DISPLAY CIRCUIT OF RECEIVED FREQUENCY

The block diagram of the display circuit is shown in Fig. 9.

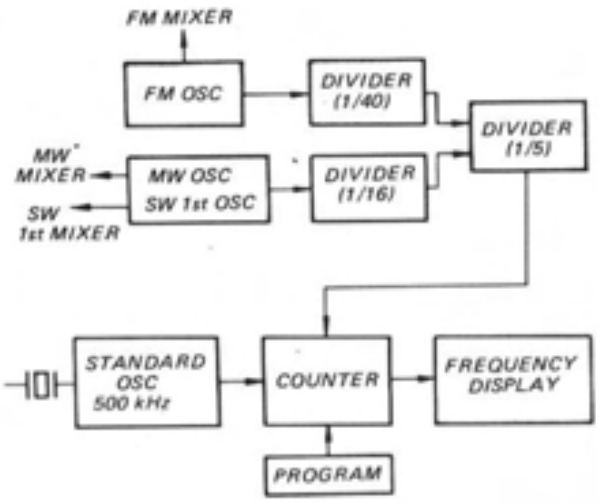


Fig. 9

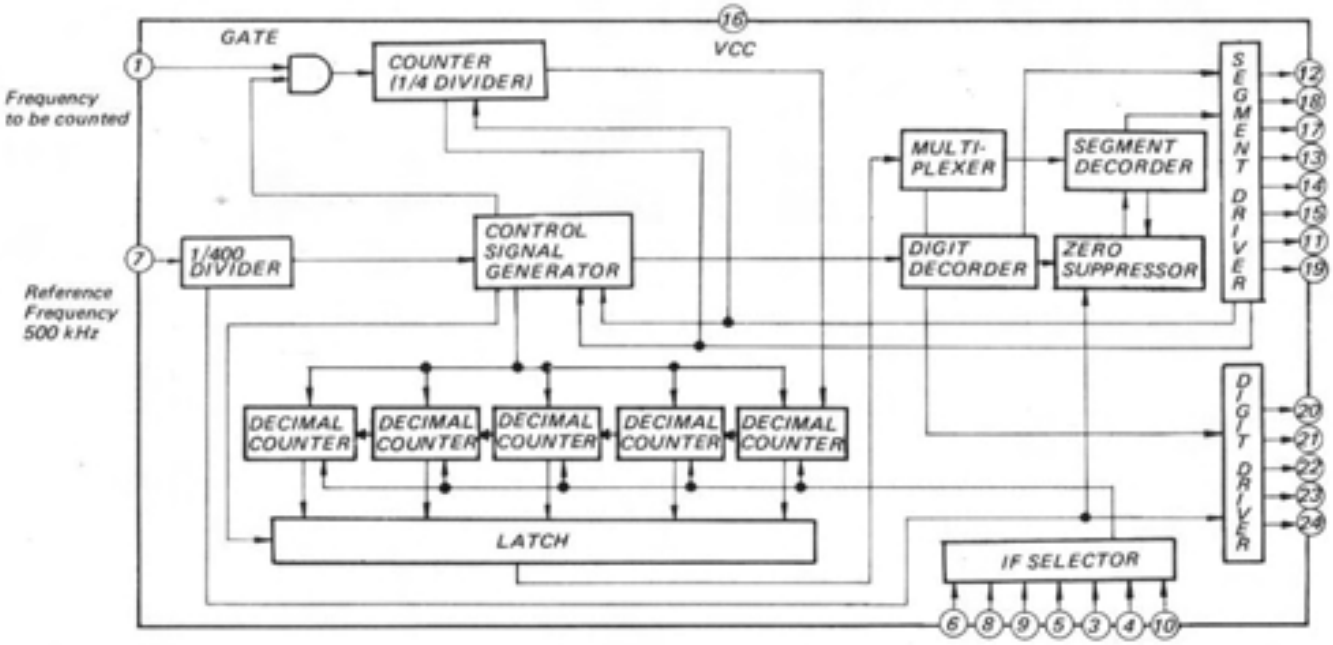


Fig. 10 BLOCK DIAGRAM OF IC 6

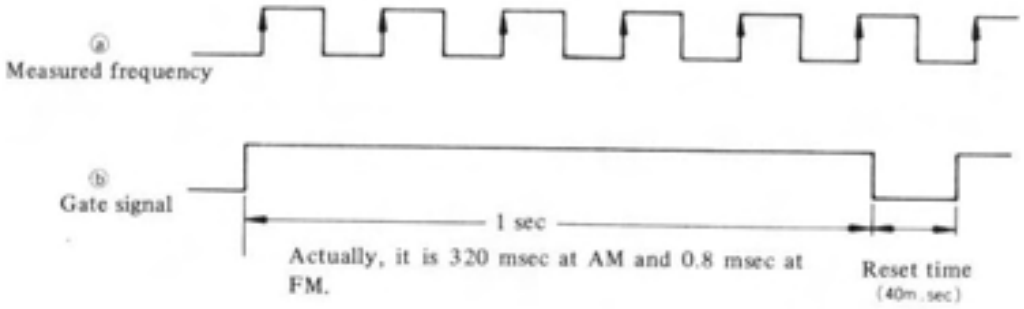


Fig. 11

Basic Operation of IC6 Counter

When a signal whose frequency is to be measured is applied to terminal 1, this signal enters the gate circuit. A reference frequency of 500 kHz is generated at terminal 7, and this signal is applied to the control-signal generator through the divider.

This signal is divided further in the control-signal generator so that a pulse lasts for a second as shown in Fig. 11. Actually, a display down to 1 kHz in AM and 100 kHz in FM is sufficient. Thus, pulses in AM and in FM are set to be 320 msec and 0.8 msec respectively. This signal from the control-signal generator, is applied to the gate circuit (this signal is referred to as the gate signal). The gate circuit acts as an AND circuit, and an output signal appears when both ⓐ and ⓑ are at the same level. This output signal is divided and counted by the decimal counter.

As shwon in Fig. 11, 6 pulses counted for a duration of 1 second make up the frequency 6 Hz.

Actually, high frequencies on the order of 10 MHz are received. Since the gate signal lasts for a second, the decimal counter must count pulses on the order of 10^5. Therefore, an extremely high speed counter is essential. The gate signal and the frequency to be measured are divided at the same proportion and counted. This method is called "Prescaling".

Decimal Counter

The signal generated above is applied to the decimal counter and its frequency is counted. The decimal counter returns to 0 after counting from 0 to 9, and 1 is displayed at the next counter.

Explanation of the operation of the decimal counter will be given using an example of a decimal counter in the Master-Slave system (negative-going trigger).

In this method as shown in Fig.12, the counter reads in the signal while the input signal is at a higher level, as indicated by the heavy line, and generates signals according to the truth table in Fig.13 when the input signal changes from the higher to the lower level as indicated by the arrow.

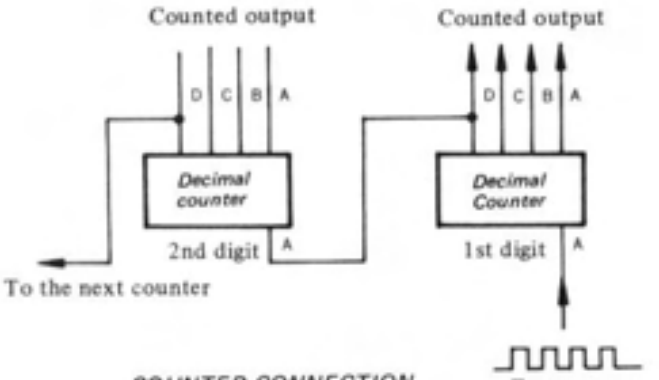
Fig. 12

Truth Table

Count	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Return from 9 to 0.

Fig. 13



COUNTER CONNECTION
Fig. 14

The frequency to be measured is applied to input A. Output D is connected input A of the next counter, and the next counter displays 1 when the count changes from 9 to 10.

Output D becomes 1 at 8 in the table, but the next counter does not display 1. The reason for this is that the signal to input A of the next counter is at a high level for both 8 and 9 and only goes low when the signal changes to a low level after 9.

The frequency is measured by using this technique.

The signals (outputs from A, B, C, D mentioned above) from the decimal counters are simultaneously sent to the latch circuit.

When the gate signal goes off, the decimal counter is reset to 0 for the next counter.

Latch Circuit

The result of the decimal count is put in the memory of the latch circuit when the gate signal is terminated. The purpose of the latch circuit is to keep certain information for a certain period of time.

In general, the latch circuit is made up of D type flip-flops.

Without the latch circuit, the display of the counter changes constantly as the counter counts pulses while the gate is open. The display becomes fixed and readable only when the gate is closed. The display returns to 0 when a reset signal is received and starts counting as the gate opens. This operation is repeated.

Therefore, with the latch circuit the display is fixed when the counting is over and continues to be so even when the reset signal is received. The display changes to show the results of the next count only when the next count is finished.

Multiplexer

The signal from the latch circuit is then sent to the multiplexer. This IC controls the LED display unit by a method called "dynamic drive", the generation of pulses to illuminate the digits of the LED in order from the 1st to the 5th digit.

Each digit of the LED is lit in sequence at a fast rate, but appears to the human eye to be lit continuously due to the "persistence of vision" effect.

This operation is performed through the multi-

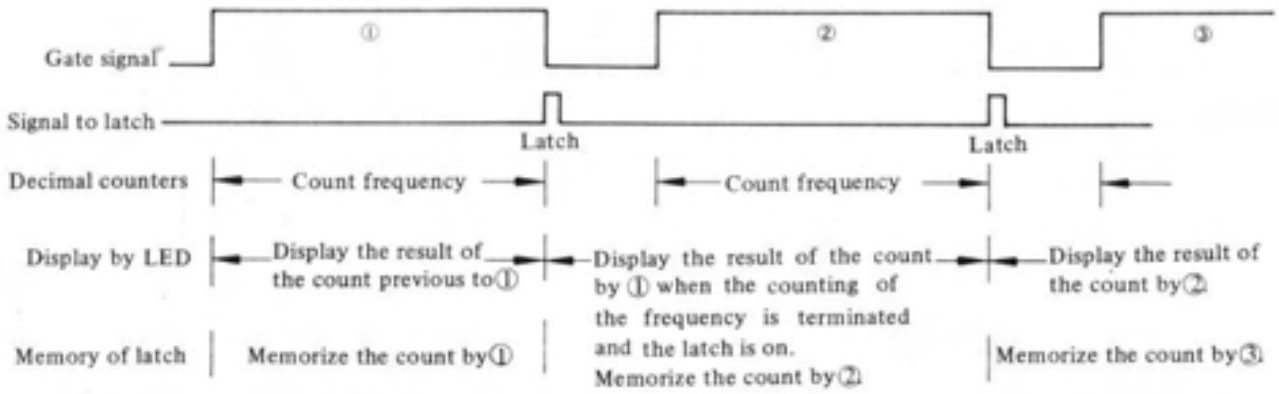
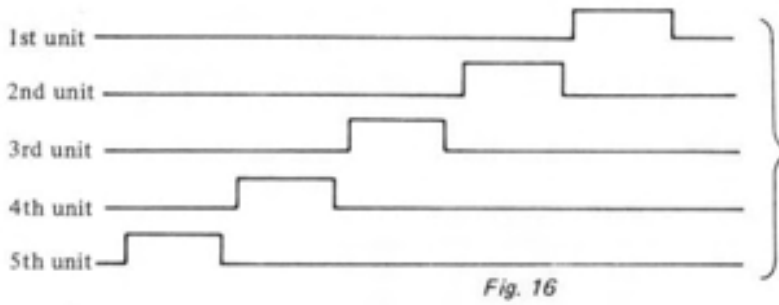


Fig. 15

The same segment in each unit is connected in parallel.



Apply a pulse so that each unit lights up in sequence.

Fig. 16

Segment Decoder

The purpose of the segment decoder is to change the output signals of the decimal counter to signals that illuminate the corresponding segment (a–g) of the LED.

The segment decoder operates as shown below. When the figure "2" is desplayed, for example, the signals shown in Fig. 8 are sent as output signals from the segment decoder.

Display of figure "2"

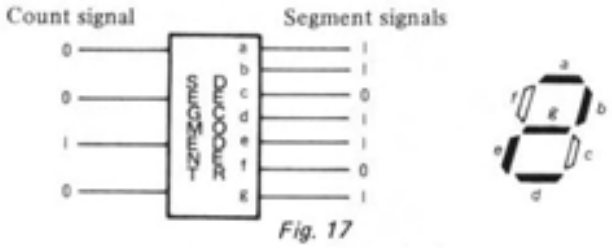


Fig. 17

Conversion Table

Figure	Count signal	Segment signal						
		a	b	c	d	e	f	g
0	0 0 0 0	1	1	1	1	1	1	0
1	0 0 0 1	0	1	1	0	0	0	0
2	0 0 1 0	1	1	0	1	1	0	1
3	0 0 1 1	1	1	1	1	0	0	1
4	0 1 0 0	0	1	1	0	0	1	1
5	0 1 0 1	1	0	1	1	0	1	1
6	0 1 1 0	1	0	1	1	1	1	1
7	0 1 1 1	1	1	1	0	0	1	0
8	1 0 0 0	1	1	1	1	1	1	1
9	1 0 0 1	1	1	1	1	0	1	1

Segment Driver

This amplifies signals generated by the segment decoder to the level required to operate the LED segments.

Digit Decoder

This generates signals for the multiplexer and the digit driver simultaneously.

Digit Driver

As previously mentioned in the explanation of the multiplexer, this IC provides the "dynamic drive" for the LED display.

This illuminates the 1st to the 5th digits in order. Q41–45 control the on-off operations of each digit of the LED. On-off signals are sent to Q41–45 by the digit driver.

Zero Suppress

Zero suppress is the circuit which terminates the display of zeroes preceding the significant figure.

Example: 00100 kHz
└─These 00 figures are not displayed.

Dynamic chart of each signal

An output dynamic chart for 12345 is given below as an example.

When both digit and segment outputs are at High level, the output is on.

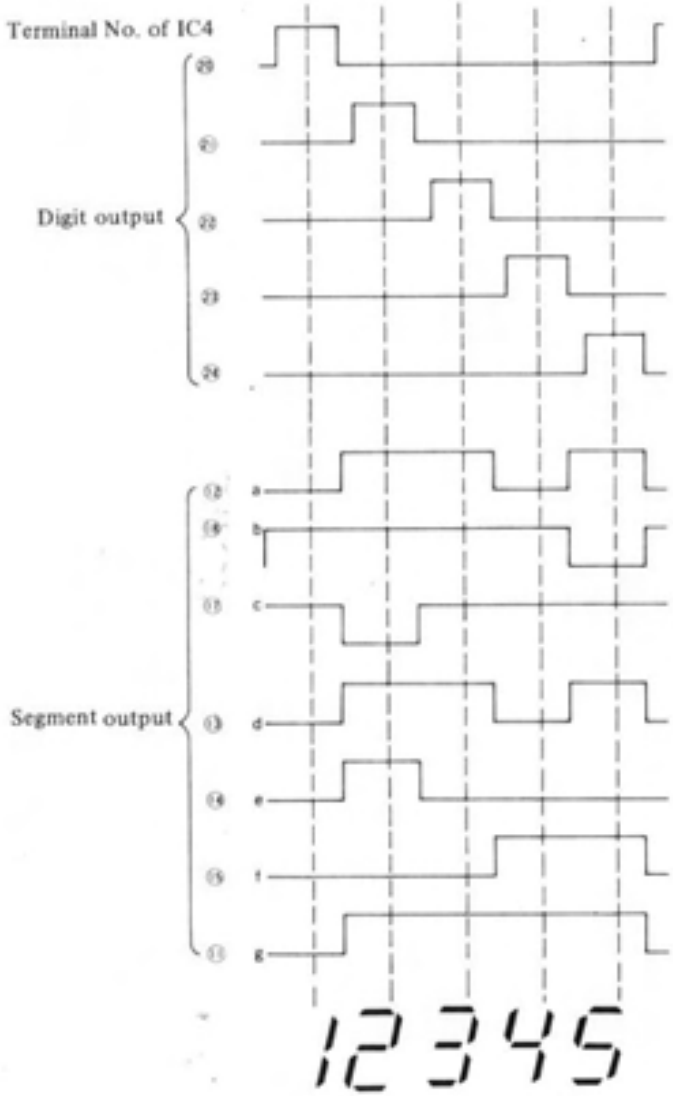


Fig. 18

I-F Selector

Since the frequency of the first local oscillator is 20.7 MHz, the counter would indicate 20.7 MHz if counted as it is, even if one wishes to display 10 MHz when receiving SW.

In order to get a display of 10 MHz a certain frequency must first be subtracted from the local-oscillator frequency. The I-F selector performs this subtraction. The counter has a display of five digits. If 0000 is set to be displayed when 10.700 is applied, 00001 kHz is displayed when 10.701 MHz is measured.

In order to get this performance, 10700 should be subtracted from the decimal counter before the next count.

These figures are calculated as follows.

100000 − 10700 = 89200

6 units

The figures 89200 should be set in the counter before counting a given frequency.

When 10.700 is counted, the display of the counters becomes 0, since 10700 + 89200 = 100000.

1 in the sixth digit is not displayed, since only 5 figures are displayed.

The I-F selector selects the figures to set in the counter before counting. The following figures are set by the I-F selector in this system.

FM	89200	
MW	99545	
SW	89200	(WIDE, NARROW)
	89198	(USB)
	89202	(LSB)

For SSB receivers, the received frequency is set at the carrier position. However, the oscillation frequency of transmitter is 2 kHz above or below the carrier frequency, and thus the I-F selector adds or subtracts 2 kHz before counting.

Timing chart of each signal

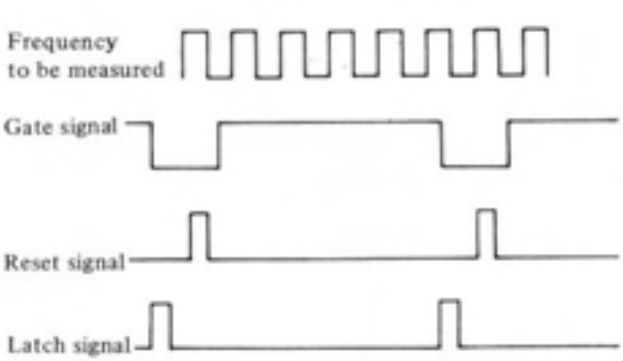


Fig. 19

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K4XL's  BAMA

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